WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer, the fin having a plurality of side surfaces, a top surface and a bottom surface; and

a gate formed on the insulating layer, the gate surrounding the plurality of side surfaces, the top surface and the bottom surface of the fin at a channel region of the semiconductor device.

2. The semiconductor device of claim 1, wherein the gate comprises a first gate disposed on a first side of the fin and a second gate disposed on a second side of the fin opposite the first side.

3. The semiconductor device of claim 2, wherein a portion of the gate surrounding the bottom surface of the fin comprises a third gate.

4. The semiconductor device of claim 3, wherein a portion of the gate surrounding the top surface of the fin comprises a fourth gate.

5. The semiconductor device of claim 1, further comprising:

a first dielectric layer formed around the plurality of side surfaces and the bottom surface of the fin.

6. The semiconductor device of claim 5, further comprising:

at least one dielectric layer formed over the top surface of the fin.

7. The semiconductor device of claim 6, wherein the at least one dielectric layer comprises:

an oxide layer formed over the top surface of the fin, and

a nitride layer formed over the oxide layer.

8. The semiconductor device of claim 7, wherein the first dielectric layer has a thickness ranging from about 8 Å to about 50 Å, the oxide layer has a thickness ranging from about 20 Å to about 400 Å and the nitride layer has a thickness ranging from about 100 Å to about 800 Å.

9. The semiconductor device of claim 1, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin, wherein the insulating later comprises a buried oxide layer and the fin comprises at least one of silicon and germanium.

10. A method of manufacturing a semiconductor device including, comprising:

forming at least one dielectric layer over a silicon on insulator (SOI) wafer, the SOI wafer comprising a conductive layer on an insulating layer that is formed on a substrate;

forming a mask over the at least one dielectric layer;

etching the at least one dielectric layer;

etching a portion of the conductive layer to form a fin structure, the fin structure having a plurality of side surfaces, a top surface and a bottom surface, wherein a lower portion of the fin structure has a narrower width than a top portion of the fin structure;

etching a remaining portion of the conductive layer to laterally undercut the conductive layer located below the fin structure;

forming a gate dielectric on the plurality of side surfaces and bottom surface of the fin structure;

depositing a gate material over the fin structure, the gate material surrounding the plurality of side surfaces, the top surface and the bottom surface of the fin structure; and

patterning and etching the gate material to form a gate electrode, the gate electrode surrounding the plurality of side surfaces, the top surface and the bottom surface of the fin structure in a channel region of the semiconductor device.

11. The method of claim 10, further comprising:

forming source and drain regions adjacent the end portions of the fin structure;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

12. The method of claim 10, wherein the etching a remaining portion of the conductive layer comprises:

using HBr to remove the lower portion of the fin structure.

13. The method of claim 10, wherein the forming at least one dielectric layer comprises:

forming a first dielectric layer over the SOI wafer, the first dielectric layer having a thickness ranging from about 20 Å to about 400 Å, and

forming a second dielectric layer over the first dielectric layer, the second dielectric layer having a thickness ranging from about 100 Å to about 800 Å.

14. The method of claim 13, wherein the first dielectric layer comprises an oxide and the second dielectric layer comprises a nitride.

15. A semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end, a second end and a middle portion located between the first and second ends, wherein the first and second ends are disposed on the insulating layer and the middle portion is separated from the insulating layer;

at least one dielectric layer formed over a top surface of the conductive fin;

a gate dielectric layer formed on side surfaces and a bottom surface of the conductive fin; and

a gate formed on the insulating layer, the gate surrounding the gate dielectric layer formed on the side surfaces and bottom surface at the middle portion of the conductive fin and covering the at least one dielectric layer formed over the top surface at the middle portion of the conductive fin.

16. The semiconductor device of claim 15, wherein the gate comprises a first gate electrode disposed on a first side of the conductive fin and a second gate electrode disposed on an opposite side of the conductive fin.

17. The semiconductor device of claim 16, wherein the gate further comprises a third gate electrode disposed on a bottom side of the conductive fin.

18. The semiconductor device of claim 17, wherein the gate further comprises a fourth gate electrode disposed on a top side of the conductive fin.

19. The semiconductor device of claim 15, wherein the at least one dielectric layer comprises:

an oxide layer having a thickness ranging from about 20 Å to about 400 Å, and

a nitride layer having a thickness ranging from about 100 Å to about 800 Å.

20. The semiconductor device of claim 15, further comprising:

a source region and a drain region formed above the insulating layer and adjacent a respective first and second end of the fin, wherein the gate dielectric layer has a thickness ranging from about 8 Å to about 50 Å.